AMENDMENTS

IN THE CLAIMS:

Please amend claims 8, 17, and 24, cancel claims 26-27, and add new claims 30-31 as provided below:

1-7. (Canceled)

8. (Currently Amended) An ingress/egress port for an Ethernet switch comprising:

a plurality of Media Access Control (MAC) interfaces, each MAC interface is configured to receive/transmit Fast Ethernet (FE) packets, at least one of the MAC interfaces further being configured to receive/transmit Gigabit Ethernet (GE) packets independent of the other plurality of MAC interfaces;

receive and transmit modules which are configured respectively to receive both GE and FE packets from, and transmit both GE and FE packets to, all the MAC interfaces; and

wherein the ingress/egress port operates as a single GE port in a first mode of operation and as more than one FE port in a second mode of operation; and

wherein each MAC interface is associated with a separate buffer configured to store packets as they are received at the respective MAC interface, the receive module being arranged to receive packets from the respective buffers sequentially.

9. (Previously Presented) The ingress/egress port according to claim 8 wherein only one of the MAC interfaces is configured to receive/transmit both GE and FE packets, the other MAC interfaces only being adapted to receive/transmit FE packets.

10. (Previously Presented) The ingress/egress port according to claim 9 wherein the receive module receives the FE packets sequentially even if FE packets actually reach different ones of the MAC interfaces simultaneously.

11. (Previously Presented) The ingress/egress port according to claim 8 wherein the receive module receives the FE packets sequentially even if FE packets actually reach different ones of the MAC interfaces simultaneously.

12. (Previously Presented) The ingress/egress port according to claim 8 wherein the receive module further includes a memory configured to store packet data, and a receiver interface configured to extract header data from the packet data and generate a descriptor therefrom, the descriptor associated with the packet data within the receive module.

13. (Previously Presented) The ingress/egress port according to claim 12, wherein the receive module further comprises a set of buffers configured to receive packets from at least one of the MAC interfaces, and wherein the receiver interface is further configured to fetch packet data from the set of buffers and store the packet data in the memory.

14. (Previously Presented) The ingress/egress port according to claim 13, wherein each buffer of the set of buffers comprises a first-in-first-out buffer.

15. (Previously Presented) The ingress/egress port according to claim 13, wherein the receiver interface is further configured to store the descriptor associated with the packet data in the memory.

16. (Previously Presented) The ingress/egress port according to claim 8 wherein the plurality of MAC interfaces consists of 8 MAC interfaces.

17. (Currently Amended) An Ethernet switch comprising:

at least one ingress/egress port, each ingress/egress port having

a plurality of Media Access Control (MAC) interfaces, each MAC interface is configured to receive/transmit Fast Ethernet (FE) packets, at least one of the MAC interfaces further being configured to receive/transmit Gigabit Ethernet (GE) packets independent of the other plurality of MAC interfaces;

receive and transmit modules which are configured respectively to receive both GE and FE packets from, and transmit both GE and FE packets to, all the MAC interfaces; and

wherein the ingress/egress port operates as a single GE port in a first mode of operation and as more than one FE port in a second mode of operation; and

wherein each MAC interface is associated with a separate buffer configured to store packets as they are received at the respective MAC interface, the receive module being arranged to receive packets from the respective buffers sequentially.

18. (Cancelled)

19. (Previously Presented) The Ethernet switch according to claim 17, wherein the at least one ingress/egress port comprises eight ingress/egress ports, each ingress/egress port being configured to switch between a first mode and a second mode, in which each ingress/egress port operates as a single GE port in the first mode and as eight FE ports in the second mode and wherein the switch can operate as *n* GE ports and *8(8-n)* FE ports for *n* a selectable integer in the range 0 and 8.

20. (Previously Presented) The Ethernet switch according to claim 17, wherein the receive module further includes a memory configured to store packet data, and a receiver interface configured to extract header data from the packet data and generate a descriptor therefrom, the descriptor associated with the packet data within the receive module.

21. (Previously Presented) The Ethernet switch according to claim 20, wherein the receive module further comprises a set of buffers configured to receive packets from at least one of the MAC interfaces, and wherein the receiver interface is further configured to fetch packet data from the set of buffers and store the packet data in the memory.

22. (Previously Presented) The Ethernet switch according to claim 21, wherein each buffer of the set of buffers comprises a first-in-first-out buffer.

23. (Previously Presented) The Ethernet switch according to claim 21, wherein the receiver interface is further configured to store the descriptor associated with the packet data in the memory.

24. (Currently Amended) A method, comprising

providing data packets to an ingress/egress port of an Ethernet switch, ingress/egress port having a plurality of Media Access Control (MAC) interfaces, each MAC interface configured for receiving/transmitting Fast Ethernet (FE) packets, at least one of the MAC interfaces further being configured to receive/transmit Gigabit Ethernet (GE) packets independent of the other plurality of MAC interfaces;

storing the data packets in buffers associated with the plurality of MAC interfaces, each MAC interface being associated with a separate buffer;

passing packet data from the data packets from the buffers to a receive module, the receive module configured to receive both GE and FE packets from all the MAC

interfaces;

passing outgoing packet data from a transmit module to the MAC interfaces, the transmit module configured to transmit both GE and FE packets to all the MAC interfaces; and

switching the ingress/egress port between a first mode and a second mode, in which the ingress/egress port operates as a single GE port in the first mode and as more than one FE port in the second mode.

25. (Previously Presented) The method according to claim 24, further comprising providing a control signal to determine whether the MAC interfaces operate as FE interfaces or whether the at least one MAC interface operates as a GE interface.

26. (Cancelled).

27. (Cancelled).

28. (Previously Presented) An ingress/egress port for an Ethernet switch, the ingress/egress port comprising:

a plurality of Media Access Control (MAC) interfaces, each MAC interface being configured to receive/transmit Fast Ethernet (FE) packets, at least one of the MAC interfaces further being configured to receive/transmit Gigabit Ethernet (GE) packets;

receive and transmit modules which are configured respectively to receive both GE and FE packets from, and transmit both GE and FE packets to, all the MAC interfaces; and

a switch configured to switch the ingress/egress port between a first mode and a second mode of operation for the ingress/egress port, wherein the ingress/egress port operates as a single GE port in the first mode of operation using the at least one of the MAC interfaces to transmit and receive GE packets and as more than one FE port in the second mode of operation using the plurality of MAC interfaces to transmit and

receive FE packets.

29. (Previously Presented) An ingress/egress port for an Ethernet switch, the ingress/egress port comprising:

a plurality of Media Access Control (MAC) interfaces configured to receive/transmit Fast Ethernet (FE) packets;

at least one MAC interface configured to receive/transmit Gigabit Ethernet (GE) packets in a first mode of operation and to receive/transmit FE packets in a second mode of operation; and

receive and transmit modules which are configured respectively to receive both GE and FE packets from, and transmit both GE and FE packets to, all the MAC interfaces;

wherein the ingress/egress port operates as a single GE port in the first mode of operation using the at least one MAC interface to transmit and receive GE packets and as more a plurality of FE ports in the second mode of operation using the plurality and the at least one MAC interface to transmit and receive FE packets.

30. (New) The ingress/egress port according to claim 14, the receive module further comprising:

a parser for extracting information from headers in the received packets, and adding this information to the descriptor.

31. (New) The ingress/egress port according to claim 30,

wherein the receive parser is configured to extract eight 2-byte items from each received data packet, wherein the 2-byte items are written to the first 16 bytes of a memory bank, and

wherein the extraction is performed based upon offsets programmed into offset registers of a register file.